FIG 1

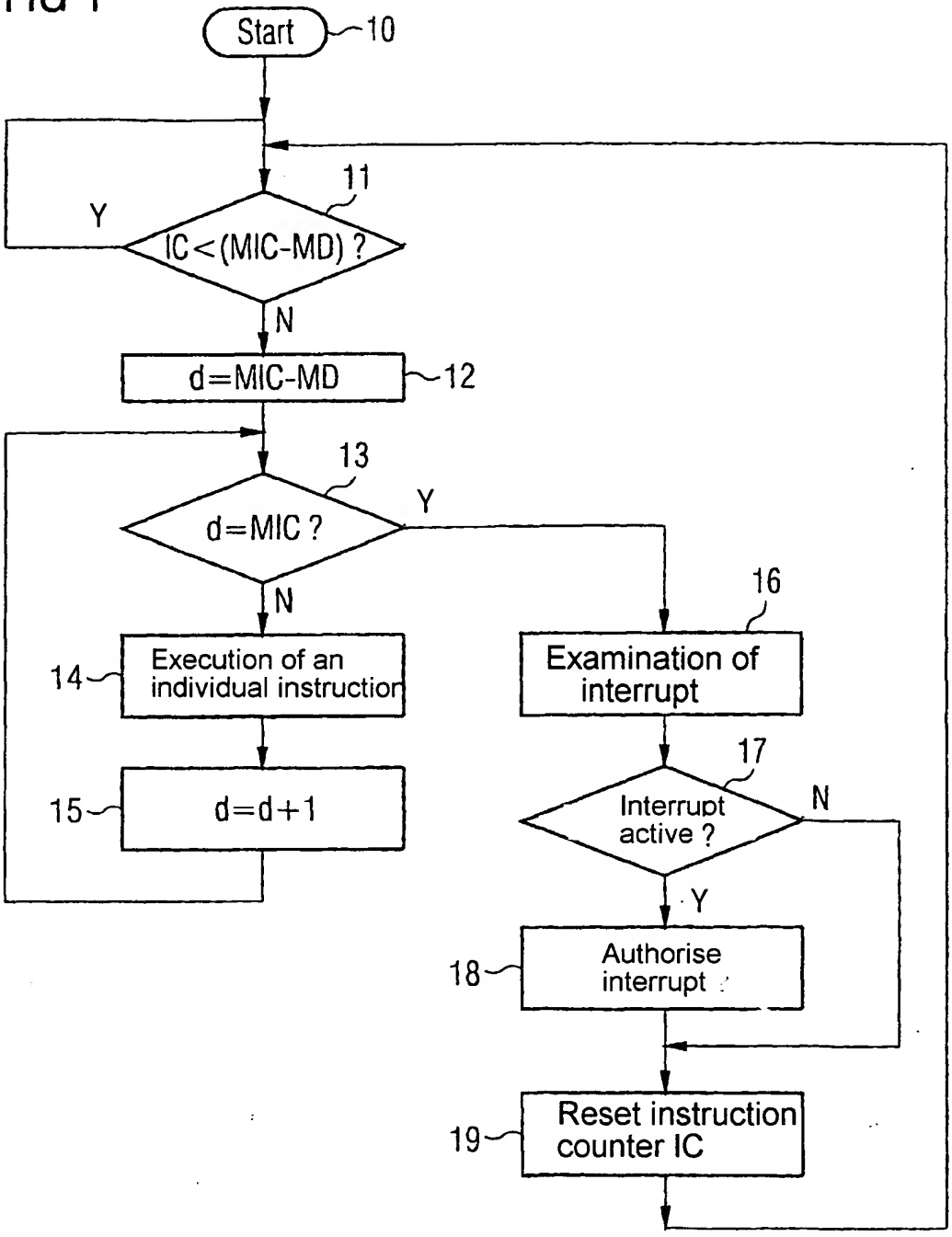

Start
10
11
Y
IC<(MIC-MD) ?
N
d=MIC-MD
12
13
d=MIC ?
Y
N
16
14
Execution of an individual instruction
Examination of interrupt
17
15
d=d+1
Interrupt active ?
N
Y
18
Authorise interrupt
19
Reset instruction counter IC

FIG 2

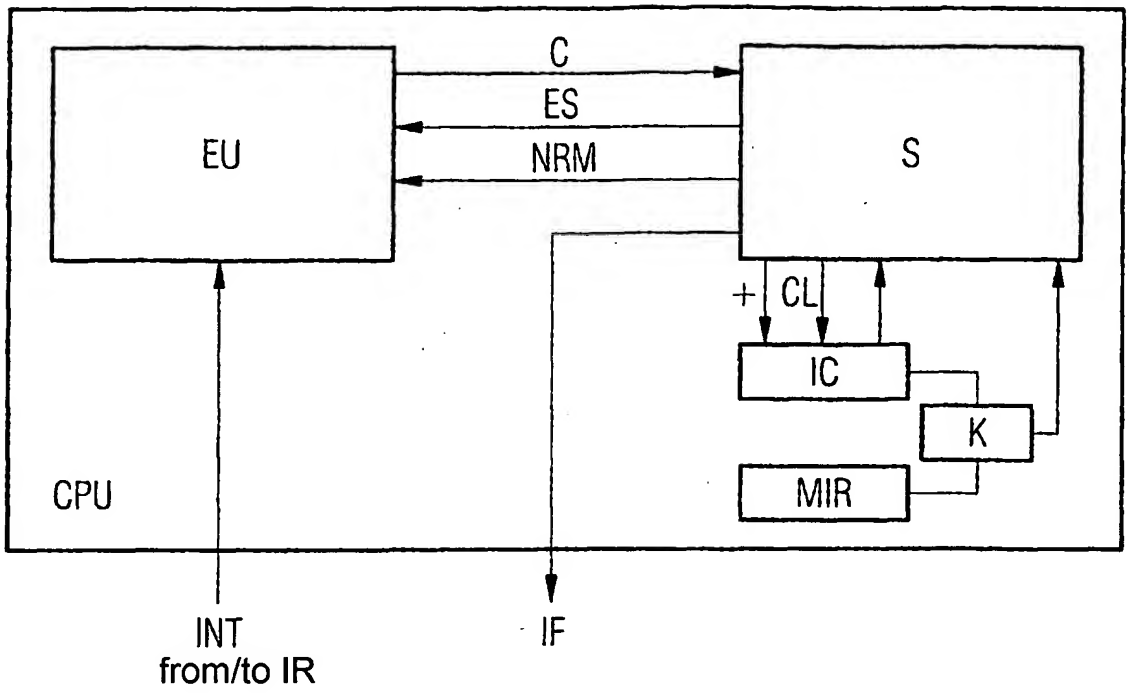
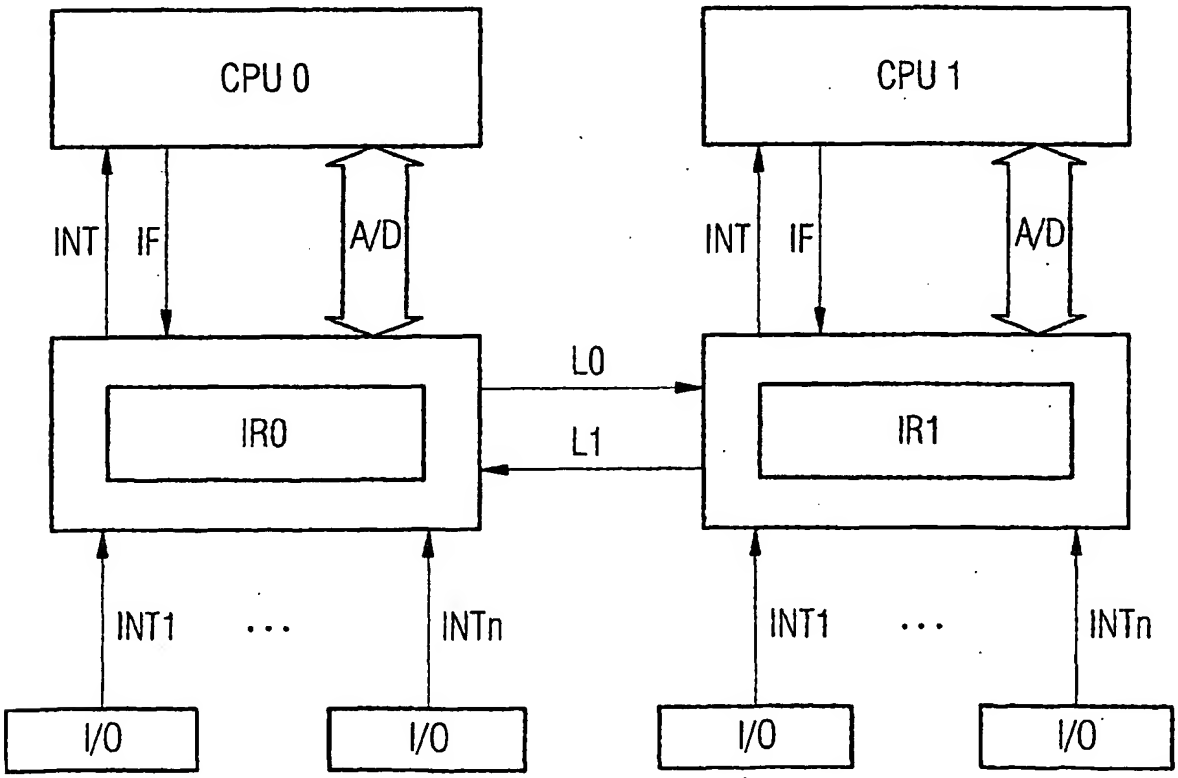

C
ES
NRM
EU
S
+
CL
IC
K
MIR
CPU
INT
from/to IR
IF

FIG 3


CPU 0
CPU 1
INT
IF
A/D
INT
IF
A/D
L0
L1
IR0
IR1
INT1
INTn
INT1
INTn
I/O
I/O
I/O
I/O